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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,827	WEIMER, RONALD A.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62 and 78-157* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-62 and 78-157* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/01, 12/03/02.*) 9/4/03, 1/13/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Response dated 09/01/2005.

Election/Restrictions

1. Restriction requirement dated 08/08/2005 has been withdrawn since based on Applicant's application, the polysilicon substrate in claims of group I invention is the same as a electrode comprising polysilicon layer in claims of group II. Accordingly, claims 1-62 and 78-157 are examined in merit.

Oath/Declaration

2. Oath/Declaration filed on 08/29/2001 has been acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 43-62, 95-100, 105-110, 125-127, 130, 132-137 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

► With respect to claim 43, "the electrode" lacking antecedent basis should be changed to "the lower electrode"

► With respect to claim 45, "the dielectric layer" lacking antecedent basic should be changed to "the high K dielectric layer"

► With respect to claim 46, "the electrode" lacking antecedent basis should be changed to "the lower electrode"

► With respect to claim 48, "the electrode" lacking antecedent basis should be changed to "the first capacitor electrode"

► With respect to claims 49 and 50, "the dielectric material" lacking antecedent basis should be changed to "the dielectric layer"

► With respect to claim 53, "the electrode" lacking antecedent basis should be changed to "the first capacitor electrode"

► With respect to claim 54, "the electrode" lacking antecedent basis should be changed to "the lower electrode"

► With respect to claim 55, "the polysilicon electrode" lacking antecedent basic should be changed to "the lower electrode comprising polysilicon"

► With respect to claim 56, "the electrode" lacking antecedent basis should be changed to "the lower electrode"

► With respect to claim 57, "the first electrode layer" and "the electrode" lacking antecedent basis should be changed to "the first conductive electrode layer"

► With respect to claim 61, "annealing the layer..." renders the claim indefinite. It is not clear with layer is annealed.

► With respect to claims 95, "the polysilicon lower electrode" lacking antecedent basis should be changed to "the conductive polysilicon lower electrode"

► With respect to claim 96, "the polysilicon electrode" lacking antecedent basis should be changed to "the first electrode comprising polysilicon"

► With respect to claims 97-99, "the polysilicon electrode" lacking antecedent basis should be changed to "the first electrode comprising polysilicon". In addition, "the dielectric layer" lacking antecedent basis should be changed to "the high K dielectric layer".

► With respect to claim 100, "the dielectric layer" lacking antecedent basis should be changed to "the high K dielectric layer"

► With respect to claims 105-110, it is not clear how the substrate can be within the one or more openings when the one or more openings are in the insulative layer and extend to the substrate. Moreover, "the polysilicon electrode" lacking antecedent basis should be changed to "the first electrode comprising polysilicon". In addition, "the dielectric layer" lacking antecedent basis should be changed to "the high K dielectric layer".

► With respect to claim 125, it is not clear where "a semiconductor substrate" comes from and is located.

► With respect to claims 126-127, it is not clear if there is any relationship between "a polysilicon layer" is "the polysilicon substrate" or not.

► With respect to claim 130, it is not clear if there is any relationship between "a layer of polysilicon" and "the polysilicon substrate" or not

► With respect to claim 132, it is not clear if there is any relationship between "a first conductive electrode" and "the polysilicon substrate" or not (see figs 1-2, the first

conductive electrode 18 is the same as the polysilicon substrate that is thermally annealed in nitric oxide to form the oxynitride in fig. 2). In addition, "the first electrode" lacks antecedent basic.

► With respect to claims 134-137, "the second electrode" lacks antecedent basic.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-8, 11-28, 30-32, 35-56, 78-80, 83-86, 89-100, 102, 104-112, 114-123, 125-131, 138-142, 145-151, 156-157, as being best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Wallace et al [US 2001/0024853].

****Notice**: these rejections are based on broad scope of the claims wherein annealing polysilicon in nitric oxide (nitric oxide is a type of nitrogen gas) and nitridizing by thermal annealing in nitrogen gas can be considered as a single step or respectively considered as a begin of the step of oxynitridation polysilicon and an ending of the step of oxynitridation polysilicon. The silicon oxynitride is considered a type of an oxide layer, a nitride layer, a nitrided oxide layer and a silicon nitride layer as claimed.*

► With respect to claims 1-8, 11-28, 30-32, 35-40, 78-80, 83-86, 89-94, 111-112, 114-123, 125-131, 138-142, 145-147, 150-151 and 156-157, Wallace et al (figs 1-7's, abstract and text pages 1-5) disclose a method for forming a dielectric layer comprising:

providing a semiconductor substrate (fig 7c) comprising an insulative layer (62, fig 7d) disposed thereon;

forming one or more openings in the insulating layer (62) extending to the semiconductor substrate (fig 7c);

providing a polysilicon substrate (30, fig 7g) over the semiconductor substrate and within the one or more openings, the polysilicon substrate comprising a capacitor electrode, the polysilicon :

annealing the polysilicon substrate (abstract, text [0042], [0025]-[0028] & [0045]) in a nitric oxide at a temperature about 700 to about 750°C (e.g. 700°C, text [0025]) to form the an oxynitride layer layer (an oxynitride/oxide 25 initially formed) wherein nitrogen would concentrates within the oxynitride layer which is an oxide layer, the oxynitride layer (the oxyinitrie/oxide 25 initially formed) inherently having a thickness of about 15 angtroms or less ;

nitridizing the oxynitride layer to form a nitride layer by thermal annealing and exposing the oxynitride layer to activated nitrogen gas of nitric oxide (text [0025]-[0028] & [0045]: *the initially formed silicon oxynitride 25 is continued to be nitridized by the NO wherein the NO is activated by temperature of annealing of 700°C*), wherein the oxynitride layer and the nitride layer have a combined thickness of about 10 angstroms (text [0028])

depositing a dielectric layer of high k dielectric of tantalum pentoxide (24, fig 7i, text [0043], [0046]) onto the nitride layer/nitrided oxynitride layer;

annealing and exposing the dielectric layer (24) in an oxidizing gas (text [0046]: *the dielectric layer 24 initially formed inherently exposed to the oxidizing gas of oxygen and inherently annealed at temperature of 700oC*);

wherein upon exposing and annealing the dielectric layer (24) to the oxidizing gas, the nitrided oxynitride layer (25) inhibits oxidation of the polysilicon substrate (abstract), the oxynitride layer (25) has a thickness *substantially* the same (*can be either the same or changed*) before and after annealing the dielectric layer; and

depositing a conductive material selected from the group consisting of doped polysilicon, tungsten, tungsten nitride, titanium nitride and platinium (conductive material 26, fig 7j, text [0043] & [0031]).

► With respect to claim 41-42, Wallace et al (figs 1-7's, abstract and text pages 1-5) disclose a method of forming a semiconductor device above a semiconducting substrate having a surface comprising:

forming a nitrided oxynitride layer (25, fig 7i, text [0025]-[0028], [0042], [0045]) over a polysilicon substrate (30) by annealing the polysilicon substrate in a presence of a nitric oxide at a temperature about 700 to about 750oC to form an oxynitride layer (oxynitride 25 initially formed) and nitridizing the oxynitride layer in an activated nitrogen containing gas (text [0025]-[0028] & [0045]: *the initially formed silicon oxynitride 25 is continued to be nitridized by the NO wherein the NO is activated by temperature of annealing*), the nitrided oxynitride layer having a thickness about 40 angstroms or less (text [0028]); and

forming a dielectric layer (24, fig 7i, text [0043], [0046]) over the nitrided oxynitride layer, wherein the dielectric material comprises a high k dielectric.

► With respect to claims 43-47, and 95, Wallace et al (figs 1-7's, abstract and text pages 1-5) disclose a method of forming a dielectric layer (24) in a capacitor container comprising an opening in an insulative layer (62) and a conductive polysilicon lower electrode (30) disposed within the opening, the method comprising steps of:

forming an oxynitride layer over the conductive polysilicon lower electrode by annealing and exposing the conductive polysilicon lower electrode (30) in nitric oxide at a temperature about 700 to about 750°C, the oxynitride layer having a thickness less than 15 angstroms (text [0028]);

nitridizing the oxynitride layer in an activated nitrogen containing gas (text [0025]-[0028] & [0045]: *the initially formed silicon oxynitride 25 is continued to be nitridized by the NO wherein the NO is activated by temperature of annealing);*

forming a high k dielectric layer (24) over the nitrided oxynitride;

annealing and exposing the high k dielectric layer to an oxidizing gas (text [0046]: *the dielectric layer 24 initially formed inherently exposed to the oxidizing gas of oxygen and inherently annealed at temperature of 700oC*);

wherein the nitrided oxynitride layer (25) inhibits oxidation of the conductive polysilicon lower electrode (abstract).

► With respect to claims 48-53, 96-100, 102, 104-110, Wallace et al (figs 1-7's, abstract and text pages 1-5) disclose a method of forming capacitor comprising steps of:

providing a substrate comprising an insulating layer (62, fig 7d) disposed thereon and one or more opening in the insulative layer extending to the substrate (fig 7b);

forming a first capacitor electrode comprising polysilicon (30) over the substrate and within the one or more openings;

thermal annealing and exposing the first capacitor electrode comprising polysilicon to nitric oxide at a temperature less than about 800oC to form an oxynitride layer thereon having a thickness of about 40 angstroms or less (abstract, text [0042], [0025]-[0028] & [0045]);

thermal annealing and exposing the oxynitride layer to nitrogen gas (NO is nitrogen gas since it contains nitrogen) to nitridize the oxynitride layer (text [0042], [0025]-[0028] & [0045]: *the initially formed silicon oxynitride 25 is continued to be nitridized by the NO wherein the NO is activated by temperature of annealing*);

forming a high k dielectric layer comprising tantalum pentaoxide (24, text [0043] & [0046]) over the nitrided oxynitride layer (25);

annealing and exposing the high k dielectric layer to oxidizing gas (text [0046]: *the dielectric layer 24 initially formed inherently exposed to the oxidizing gas of oxygen and inherently annealed at temperature of 700oC*) wherein the nitridized oxynitride layer inhibits oxidation of the first capacitor electrode comprising polysilicon; and

forming a second capacitor electrode (26, fig 7j, text [0043], [0046]: evaporating aluminum) over the high k dielectric layer, the second capacitor electrode comprising a conductive material deposited by CVD or PVD (evaporizing).

► With respect to claims 54-56, Wallace et al (figs 1-7's, abstract and text pages 1-5) disclose a method of forming capacitor comprising steps of:

providing a substrate comprising an overlying insulating layer (62, fig 7d) and a container opening formed in the insulative layer to an active area of the substrate, and a lower electrode (30) comprising polysilicon formed within the container opening;

forming an oxynitride layer (an oxynitride/oxide 25 initially formed) over the lower electrode by annealing the lower electrode in a presence of nitric oxide at a temperature less than about 800oC to form an oxynitride layer thereon having a thickness of about 40 angstroms or less (abstract, text [0042], [0025]-[0028] & [0045]);

nitridizing the oxynitride layer in activated nitrogen-containing gas (text [0042], [0025]-[0028] & [0045]: *the initially formed silicon oxynitride 25 is continued to be nitridized by the NO wherein the NO is activated by temperature of annealing*);

forming a high k dielectric layer comprising tantalum pentaoxide (24, text [0043] & [0046]) over the nitrided oxynitride layer (25);

annealing and exposing the high k dielectric layer to oxidizing gas (text [0046]: *the dielectric layer 24 initially formed inherently exposed to the oxidizing gas of oxygen and inherently annealed at temperature of 700oC*) wherein the nitridized oxynitride layer inhibits oxidation of the first capacitor electrode comprising polysilicon; and

forming a second capacitor electrode (26, fig 7j) over the high k dielectric layer.

► With respect to claims 148-149, Wallace et al (figs 1-7's, abstract, text pages 1-5) discloses a method of forming a dielectric layer comprising steps of:

annealing a polysilicon substrate (30, fig 7h) in nitric oxide at a temperature of less than 800oC (text [0042], [0025]-[0028], [0045]);

nitridizing the annealed polysilicon layer to form a silicon nitride layer (text [0042], [0025]-[0028], [0045]: *the silicon oxynitride layer 25 is a silicon nitride layer is formed by oxynitridizing the annealed polysilicon in NO*);

depositing the dielectric layer (24, fig 7i, text [0043] & [0046]) onto the silicon nitride layer (25); and

exposing the high k dielectric layer to oxidizing gas (text [0046]: *the dielectric layer 24 initially formed inherently exposed to the oxidizing gas of oxygen and inherently annealed at temperature of 700oC*) wherein oxidation of the polysilicon substrate is inhibited (abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 33-34, 57-62, 101, 103, 124, 132-137 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al [US 2001/0024853] in view of Agarwal [US 6,218,256].

► With respect to claims 33-34, 57-62, 101, 124, 132-135, 137, Wallace et al substantially discloses the claimed method but does not expressly teaching using hemispherical grain polysilicon.

However, Agarwal (fig 7, col 4 lines 40-54 and col 7 lines 44-46) disclose using the hemispherical grain polysilicon (12) to increase effective area of capacitor device.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Wallace et al by using the hemispherical grain polysilicon as being claimed, per taught by Agarwal, to improve characteristic of device with reason given above.

► With respect to claims 103 and 136, tungsten, tungsten nitride, titanium nitride and platinum are known material for forming electrode. See Argawal (col 5 lines 64-67 and col 6 lines 1-15) as an evidence that shows the claimed materials as known materials for forming electrode in capacitor device. Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view Argawal, to select the claimed materials as known materials for forming the second electrode in the process of Wallace et al. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig-saw puzzle." 325 U.S. at 335, 65 USPQ at 301. See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960) (selection of a known plastic to make a container of a type made of plastics prior to the invention was held to be obvious).

6. Claims 10, 29, 81-82, 87-88, 113, 143-144 and 152 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al [US 2001/0024853] in view of Khare et al [US 6,893,979].

Wallace et al substantially discloses the claimed method but does not expressly teach exposing the oxynitride layer to a remote plasma source of nitrogen for nitridizing and plasma annealing the oxynitride layer.

However, Khare et al (figs 3's and cols 1-5) discloses exposing the oxynitride layer to a remote plasma source of nitrogen for nitridizing and plasma annealing the oxynitride layer to increase dielectric constant of the oxynitride layer.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Wallace et al by using the plasma technique as being claimed, per taught by Khare et al, to improve characteristic of the oxynitride layer with increased dielectric constant for better device performance.

7. Claims 153-155 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al [US 2001/0024853] in view of Cho [US 6,238,964].

Wallace et al substantially discloses the claimed method but is silent about saturating the dielectric layer (24) with oxygen by annealing the dielectric layer in oxygen.

However, saturating the dielectric layer with oxygen is a known and conventional technique to improve dielectric capacitance of the dielectric layer in capacitor device. See Cho (col 5 lines 52-59) as an evidence that shows saturating the dielectric layer with oxygen by annealing the dielectric layer in oxygen for improving characteristic of the dielectric layer.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Wallace et al by saturating the dielectric layer with oxygen as being claimed to improve characteristic of the dielectric layer as taught by Cho.

Allowable Subject Matter

8. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

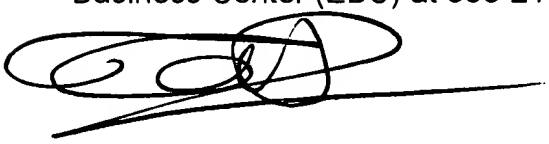
9. The following is a statement of reasons for the indication of allowable subject matter: Recorded Prior Art fails to disclose or suggest a method of forming a dielectric layer as recited in base claim 7 including annealing a polysilicon substrate in nitric oxide at a temperature of less than 800oC to form an oxynitride layer and nitridizing the oxynitride layer to form a nitride layer by exposing the oxynitride layer to a nitrogen-containing gas wherein the nitrogen containing gas is selected from the group consisting of a plasma mixture of nitrogen and helium and a plasma mixture of nitrogen and argon.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thanhha Pham